Machine Vision Standards Update
Camera Link

Steve Kinney
Director of Technical Pre-Sales
AIA Camera Link Chairman
JAI, Inc.
Camera Link Status

• Today Camera Link is the leading digital standard in factory automation worldwide

• Camera Link has added many new features in recent years. A new revision Camera Link 2.0 will be released in Nov 2011 at the Vision Show for a 45 day acceptance review.

• Camera Link HS is under development. Camera Link HS provides a quantum leap forward in bandwidth, features and performance.
Camera Link 2.0 release will consolidate:

- Mini Camera Link connectors
- PoCL – Power over Camera Link
- PoCL Lite – Smaller Minimized PoCL interface
- Appendix D – Camera Link cable specification
Camera Link 2.0

Mini Camera Link

• SDR series connectors available from 3M or Honda
• Less than ½ the height and width of standard Camera Link connectors
• Pin for pin compatibility with the full sized connectors allow interoperability with existing equipment – Fully forward + backward compatible
Appendix D – Cable Specification

- Appendix D revised the cable from a physical construction to an electrical specification
- Manufacturers build products to meet the electrical parameters and specify a maximum working distance @ 85 MHz
- This allows for a wider variety of cable assemblies for both the standard and miniature connectors, benefiting end users and system designers
Power Over Camera Link (PoCL)
A single cable solution

Pins 1 + 26, redundant grounds in legacy Camera Link equip., are isolated and may be used for either power or ground in PoCL equip.
Camera Link 2.0

Power Over Camera Link (PoCL)
A single cable solution

- Provides highest performance interface on single cable
- Fully backwards compatible - Works with powered and non-powered equipment
- Same cable assembly for both powered and non-powered equipment
- Automatic – Frame grabbers sense the powered cameras
Camera Link 2.0

PoCL Lite
A minimized solution

- Utilizes a miniature 14-pin connector
- Combines communication with data through Channel Link chipset and has only 1 control line to minimize connections
- High performance, lower cost alternative for digital conversions or upgrades to existing analog systems
Camera Link HS - Goals

• **Highest Bandwidth Solution:** Camera Link HS will need to make a quantum leap forward in bandwidth

  – Next generation will need to support data rates >32 Gb/sec (4 GBytes/sec) minimum

  – Considerations were given to architectures capable of >100 Gb/sec
Camera Link HS - Goals

• **Cable Length**: Camera Link currently supports standard cables to ~10 m. In the next revision, copper cable lengths will be increased. Considerations for low cost, fiber optic modules make distances >1000 m possible.

• **Not a Network Standard**: Camera Link HS will remain a dedicated connection. Frame grabber manufacturers can differentiate their products with support of low cost data forwarding. Cameras are to be GenICam compliant for ease of use.
Camera Link HS - Goals

• **Complete Vision Interface**: Camera Link HS will continue to incorporate low latency, real time signaling, control, and communications over the interface. Triggers and GPIO lines on the camera are controlled by the Frame Grabber. Flash strobes can be connected to the Frame Grabber, but controlled from the camera.

• **Flexibility**: Camera Link will remain a configurable digital path for data transfer between industrial cameras and PCs. This is necessary to support all the various imager resolutions and physical formats that will enter the market. For example: High-speed, multi-tap CMOS imagers.
• **Performance + Cost**: Camera Link will continue to focus on technologies that provide the market with the highest performance solutions, at the lowest cost, and with the easiest implementations for manufacturers.
Camera Link HS - Details

• Based on existing technologies and hardware – modeled around 8b/10b, K-codes, and 64/66 (10 GE) encoding.

• Physical Layer may be discrete or FPGA embedded – uses standard SERDES components which are available from both Xilinx and Altera.

• Copper CX-4 and off-the-shelf fiber optic solutions are available
FIGURE 1. In the design of the HSLINK interface, familiar Camera Link data, frame valid, line valid, and clocking signals are clocked to an FPGA (the HSLINK IP core) that is used to packetize data and provide error handling and priority requests.
Camera Link HS Features

Camera Link HS
IP Core

Packet Engine

K-Code Manager

Ext. Trigger Handler
Strobe Handler
GPIO Handler
Housekeeping
Error Handler
Camera Link HS Features

Priority Technology

- Data Resend
- Video
- Command
- GPIO
- Trigger

Priority Arbiter

Priority High

Priority Low
Data Forwarding – Allows the image to be efficiently shared, enabling the possibility of parallel processing.
In Conclusion

- Camera Link HS will build on the strengths that separate Camera Link from the other digital standards
  - High Bandwidth – 48 Gb/sec
  - Real time signaling – 32 lines - 3.2 nS minimum jitter.
  - Deterministic data transfer
  - Complete vision interface
  - Flexibility
  - Highest performance interface with the lowest cost of implementation for manufacturers
Steve Kinney
Director of Technical Pre-Sales
AIA Camera Link Chairman

JAI, Inc.
625 River Oaks Parkway
San Jose, CA 95134
USA
800-445-5444
sk@jai.com
www.jai.com
Camera Link HS Configurations and Status

Mike Miethig
Technical Manager, Teledyne DALSA
AIA Camera Link HS Chair
Participating Companies

3M
AIA Automated Imaging Association
AnaFocus
BASLER Vision Technologies
BitFlow
CEI
GIDEL
Great River Technology
Intercon 1 A Division of Nortech Systems
jAI
Matrox Imaging
Mikrotron
National Instruments
PCO Imaging
Silicon Software
Stemmer Imaging
Teledyne DALSA A Teledyne Technologies Company
teli
# Camera Link HS Release 1: Point to Point

![Diagram](image)

<table>
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<tr>
<th>MEDIA</th>
<th>NAME</th>
<th>CONNECTOR</th>
<th>UPLINK MB/s</th>
<th>DOWNLINK MB/s</th>
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<td>SFF-8470 (CX4)</td>
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Camera Link HS Release 1: Multi-Camera
Camera Link HS Release 1: Multi Frame Grabber

Bandwidth is too much for one connection and too much for one FG
Camera Link HS Release 1: Data Forwarding

Camera bandwidth is too much to process in one PC.

The unused transmitters of CX4 configuration are turned on, forwarding data to slave frame grabbers.

Framegrabber to framegrabber communication is proprietary.
Camera Link HS Release 1: Camera GPIO

32 inputs and 32 outputs are defined in the protocol, 16 are nominally reserved for camera use.

CLHS Latency ranges from 100 ns to 300 ns
Camera Link HS Release 1: Closed Loop 100 ns latency, 3.2 ns Jitter Trigger

Trigger Effectivity byte is returned in Video Header Acquisition Byte. Camera and FG will differentiate themselves on capabilities.
CLHS Timeline

• 2009 November: Teledyne DALSA debuts HSLINK - proven reliable in the field.
• 2010 April: CLHS committee formed to improve HSLINK.
• 2011 October: G3 standard
  – 45 day review period
  – Issue resolution
  – 2012 February: Final draft released
  – 2012 April: Official Release 1
Invitation

• Visit the International Standards Booth 6B73 to see early adopter products from 3M, Components Express, Mikrotron, PCO, Silicon Software, Teledyne DALSA
Mike Miethig
Technical Manager
AIA Camera Link HS Chair

Teledyne Dalsa.
605 McMurray Rd
Waterloo, Ontario
Canada
519-886-6000
mike.miethig@teledynedalsa.com
www.teledynedalsa.com