High Voltage Interfaces for CMOS/DMOS Technologies

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Abstract

This paper adapts low voltage integrated circuit (IC) design techniques to create integrated high voltage interfaces. Effective methods to implement high voltage interfaces to integrated CMOS/DMOS circuits are presented. They can be used in high voltage telecom, automotive and MEMS applications. Test results of an implemented IC show that it generates 0/100V transitions on outputs from 0/5V transitions on inputs. Test results confirm that this interface can perform a 5V/100V translation in 200 ns while driving a 32pF capacitive load.

Introduction

Advanced CMOS technology suppliers have continuously decreased supply voltages. Today, submicron technologies are typically not specified above 5V. Applications such as printer heads, serial line interface, automobile parts and MEMS are often required to operate from supply voltages above 40V. This is obviously not feasible with advanced traditional submicron CMOS.

Driven by the need to reduce the size of electronic boards and maintain high reliability, the operating supply voltage for high voltage (HV) applications are increasing steadily, ranging from 20V to 300V. Many high voltage applications require complex low voltage (LV) signal processing which greatly benefit from using submicron geometries for integration of large numbers of components (digital or analog). Ideally, dense LV CMOS should be combined with HV interfaces which interact with HV external components. Commercially available technologies supporting high voltages do not support high levels of integration. Solutions based on discrete components tend to be bulky, slow and costly.

This paper demonstrates that integrated circuits operating with supply voltages above 300V are realistic and offer good performance. It presents a design methodology that integrates HV components with LV components in order to achieve compact density, thus reducing board layout, decreasing production costs and/or increasing packaging density for the same board area. Several papers report HV integrated drivers [1], [2] and [3]. These papers propose integrated design techniques to create various high voltage interfaces. The high voltage level shifter reported here is adapted from [3]. That reference reports circuits with supply voltage of 50V. The technique and process technology presented here can be used to design circuits operating at voltages higher than 300V.

High Voltage Technology

Existing silicon foundries such as XFAB, ATMEL or AMS offer high voltage processes with either SOI or epitaxial substrates. These technologies offer a limited number of HV components for specific voltages. Some HV processes offered commercially by foundry suppliers do not always support very high breakdown voltages (i.e. >100V). DALSA Semiconductor Inc. (DALSA) offers two high voltage processes that are fully CMOS compatible. One of these processes offers submicron geometries for LV core applications. Both technologies use low-cost starting material and offers a wide range of n-type and p-type HV components with operating voltages ranging from 20V to 600V.

A. DALSA High Voltage Process Technologies

The 0.8µm and the 2µm CMOS/DMOS processes have been developed in parallel with the high voltage components. Both processes minimize the total number of process steps, while keeping low voltage portions unchanged with respect to their base technologies. A simplified HV device cross-section is shown in Fig.1. These unique HV devices exploit a lateral structure instead of a vertical one. A technique called RESURF reduces surface electrical fields. It allows increasing drain breakdown voltages up to 600 Volts. In the n-type device of Fig. 1, a P-Top region is used inside the N-Well. With carefully selected doping, the P-Top depletes at the same time as the N-Well when the drain voltage is high. It acts as a JFET in series with a conventional MOS transistor. The device families were optimized to produce a smooth field distribution when subject to high drain voltages. A significant challenge with this technology is to bring high voltages to the drain in the center of the round shaped device without adversely modifying the electric field distribution in the silicon. Metal shields must be used to preserve the desired field distribution in silicon. When a high voltage is applied to the drain, the gate to bulk potential difference is less than 10V.

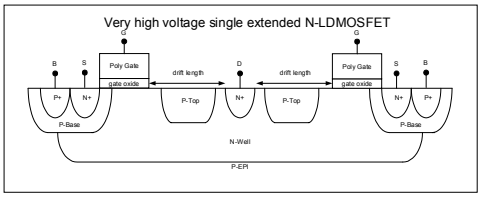

Figure 1 – Simplified cross-section view of DALSA HV LDMOSFET

Design methodologies and development

To develop a HV product, a sufficient understanding of the technology and the design methodology is required. The HV transistors are used by circuit designers as predefined cells with layout and fully characterized models and parameters. The next sections analyze DALSA technologies and how to design HV circuits.

A. Introduction to high voltage basic components

High voltage components differ from LV transistors in several ways. First the bulk connections are different. Second, when the HV transistors are in the "off" state, their drift region behaves like a pinched-off JFET device. This equivalent JFET is in series with a standard MOSFET. In spite of high drain voltages, the output leakage current through the channel of an "off" HV device has been measured to be of the order of pico Amperes (pA). When HV transistors are in the "on" state, the drift region is analogous to a low value resistor in series with the channel of a MOSFET. Simple mathematical equations describing the behavior of these HV devices are not available. The HV transistors have the same V_{GS} as LV devices. The V_{GS} of n-type HV transistors must always be smaller than 15V (nominal 5V), whereas that of p-type transistors must always be larger than –16V (nominal –5V). Therefore an HV p-type transistor with 100V power supply will have a typical gate voltage of between 95V and 100V. This is one of the most important circuit design challenges. Furthermore, since the CMOS and DMOS transistors are not built with the same layers, process variations of CMOS and DMOS devices are not matched. This is a challenge when proper operation of a circuit depends on an impedance ratio.

B. Introduction to simulation models

The purpose of the model is to emulate the behavior of the device. A model that corresponds to the I-V curve is thus acceptable, even if it is not based on the physics of how the device works. For HV devices, an intrinsic MOSFET model isn't enough. Additional sub-circuits are needed to match the actual curves. An appropriate example is the HV p-type transistors, where two different models exist for the same family. Figure 2 shows the modeled and measured responses of an HV n-type transistor that shows the quality of the fit.

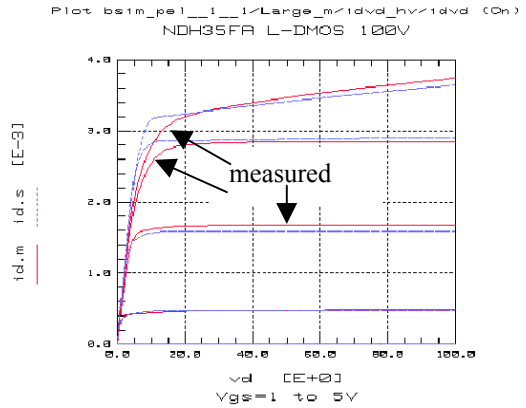

Figure 2 – Simulated vs measured Ids-Vds characteristics of a N-type HV transistor

C. Differences between DALSA 0.8µm and 2µm 5V/HV CMOS/DMOS processes

The 2µm 5V/HV process uses the same N-Well doping for the high voltage and low voltage transistors. Since this PN junction has a breakdown voltage around 150V, CMOS p-type transistors can sometimes be used in high voltage circuit configurations. This process capability gives more flexibility when designing circuits that target supplies in the order of 100V. Circuits developed using this feature cannot be transferred directly to the 0.8µm 5V/HV process. The 0.8µm 5V/HV process high voltage regions are identical to those of the 2µm process, but their low voltage regions are completely different as shown in fig.3. The 0.8µm low voltage region is a P-Well surrounded by a deep N-Well. To create the same environment as the 2µm 5V/HV process, it is possible to isolate the deep N-Well, but the PN well junction breakdown is around 50V, thus p-type LV transistors cannot be connected to the positive supply for circuits designed to operate from supplies around 100V. For circuits with complex low voltage core area, the 0.8µm 5V/HV process can result in reduced die size. However, when the LV core has minimal complexity combined with applications using supply around 100V, migration from 2µm 5V/HV to 0.8µm 5V/HV may entail some redesign, leaving the die size unchanged. In addition, yields and NREs favor the 2µm process when die sizes are comparable. Thus several factors influence the choice of the optimum technology and finer line width is not always better.

D. ESD protections

To protect the core circuitry from ESD events, suppressive devices should be implemented. However, since two voltages are present (5V/HV), more than one type of ESD protection is required. The LV pins need to be protected from each other, the HV pins need to be protected from each other, and finally, the LV pins and the HV pins need protection from each other. For the HV only, a few types of protection have been developed. Standard LV ESD protection devices are used in LV regions while HV ESD protection uses unique devices built underneath the pad to maximize density. Each ESD device was characterized individually (to evaluate breakdown characteristic, resistivity, etc) and in combination with active circuitry.

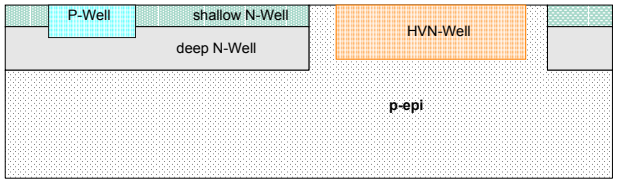

Figure 3 – Simplified cross-section view of the 0.8µm 5V/HV CMOS/DMOS process technology

Level-up shifter circuit for high voltage interfaces

Implementing a complex circuit with only a high voltage supply is usually impractical. HV transistors are much larger than LV transistors, which results in higher parasitic capacitance. Dynamic power growth is defined as CV^2, therefore the power consumption of HV gates is easily 1000 times that of LV gates. Obviously, the part of the circuit operating at HV must be minimized. With most of a circuit functionality implemented with LV circuits, a key circuit design issue is to develop effective LV-HV interfaces i.e. a level-up shifter that transforms signals from the LV core power supply domain to the HV I/O power supply domain as shown in Fig.5.

As shown in Fig. 4, the drain can support high voltages but not the gates. The two gates cannot be connected directly. Level shifting techniques have been studied in [2], [3] and applied to various high voltage supplies. The level shifter configuration proposed in [1] and [3] has been adapted to DALSA technologies. Optimisation of this circuit and the obtained results are discussed in the following sections.

A. Interconnections of high voltage components

The gate of the HV n-type transistor can be controlled by the low voltage logic levels 0 and V_{DD}, where V_{DD} is the low voltage power supply. The signal on the gate of the HV p-type transistor must be within 5V of V_{PP}, the high voltage supply. Thus conventional signals from the LV domain must be level shifted.

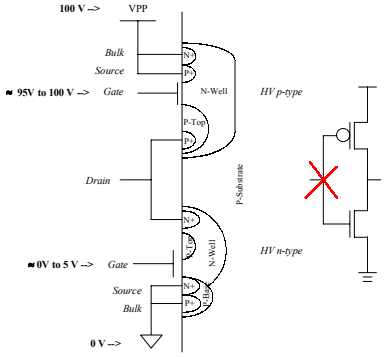

Figure 4 – Interconnections between high voltage devices

B. CMOS level shifter implementation

The adopted level-up shifter circuit is shown in Fig. 6. This circuit was chosen for its simplicity, and because it's sensitivity to process variations is second only to the output buffer. We selected the DALSA 2µm 5V/HV CMOS/DMOS technology to design a buffer that can produce 0/100V transitions at its output from 0/5V on its input.

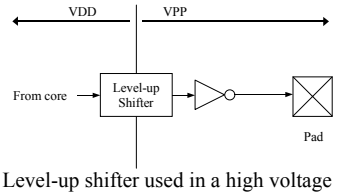

Figure 5 – Level-up shifter used in a high voltage interface

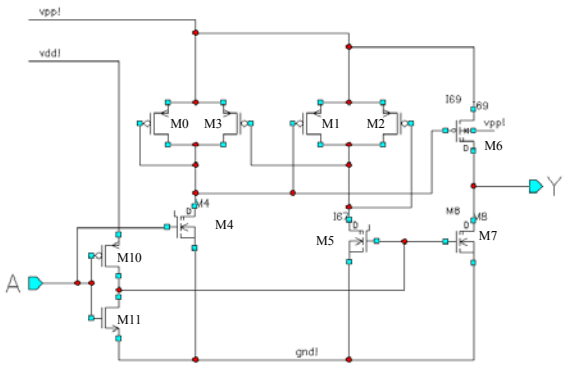

Figure 6 – Schematic of the Level-up Shifter with complementary HV output circuit.

The level-up shifter circuit is composed of transistors M0, M1, M2, M3, M4 and M5 and the output buffer is composed of M6 and M7. The inverter circuit, composed of transistors M10 and M11, is optional, and the two 5V inputs of the level shifter can use complementary internal signals. The supply voltage of the level shifter and output buffer is 100V.

C. Results and discussion

The p-type transistors within the level shifter are standard 5V devices, while the n-type transistors and the output buffer transistors are high voltage. The p-network of the level shifter needs to produce output signals from VPP to VPP-VDD. Transistors M0 and M2 are sized to limit the voltage drop on the drains of M4 and M5. Since the HV p-type transistor has a significant gate capacitance, the p-network of the level shifter must drive significant current for a short period of time to produce a short output buffer rise time. Table 1 shows simulation results of the output buffer response time for four (4) different current values in the level shifter. This table shows performance as a function of the HV devices used to implement M4 and M5. It lists the current ratings of these devices, the W/L ratio of the required M0 and M2 transistors and the RMS power dissipation value when switching a 50 pF capacitive output load in parallel with a 1Mohm resistor. Table 1 shows that configuration #2 is a good compromise between maximum frequency, power dissipation and transistor sizes. The maximum frequency was measured as the one allowing an almost full output swing (2V to 98V).

Table 1 – Level Shifter electrical characteristics

Circuit configuration number	Device name	Current rating (A)	W/L	Freq. (MHz)	Power dissip. (W)
1	NSH11EA	110.0µ	1	1.02	0.37
2	NSH12FA	1.2m	7.3	1.25	0.63
3	NDH35FA	3.5m	20.5	1.30	0.82
4	NDH11GA	11.0m	65	1.33	1.60

General Results and Discussion

Based on the previous simulation results, the configuration #2 level-up shifter was selected and implemented. Fig. 7 shows its measured characteristics.

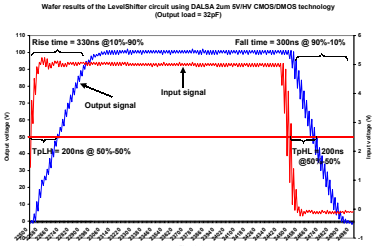

Figure 7 – Measured response of the level-up shifter

The circuit was tested with a 32pF capacitive load. Table 2 summarizes our measured test results and compares them with simulation results. By analogy to a conventional gate, the level-up shifter is characterized with respect to its input crossing $V_{DD}/2$ and its output crossing $V_{PP}/2$. The delay is measured as the time difference between the two events. Comparing the measured and simulated rise and fall times, the output buffer transistor M7, has 18% less drive than we expected, whereas transistor M6 has 21% more drive. The circuit in Fig.6 is comprised of two HV stages. The overall delay combines an internal falling transition with an output rising transition. It is hypothesized that the observed drive differences partly compensate for each other to produce balanced overall delays, even though such equal delays were not expected, based on simulations. The circuit was tested with V_{PP} ranging from 5V to 100V. It maintained its buffer functionality, and the $\partial V/\partial t$ on the output is independent of the HV power supply voltage value. The measured $(\partial V/\partial t)^{-1}$ is 3ns/V, and it is consistent with other circuits implemented with a similar configuration. In terms of ESD immunity, 1.5KV HBM (Human Body Model) was measured for fully protected circuits (with suitable ESD protection on 5V pins and HV pins). Without ESD protection on HV pins (HV output buffer not protected), the level-up shifter supported 1KV HBM. The leakage current is measured in micro (µA) amp variations after zapping. The level-up shifter occupies 51200µm^2 area and drives around 10mA.

Table 2 – Simulated and measured characteristics of the level-up shifter

Parameter	Nominal simulations results	Typical measured results	Units
Input threshold voltage transition	50	47	Volts
Output rise time @ 32pF	298	330	ns
Output fall time @ 32pF	220	300	ns
Prop. delay low-to-high @ 32pF	194	200	ns
Prop. delay high-to-low @ 32pF	134	200	ns
Output source current @ V_{OL} = 0.4V	-780	-640	µA
Output sink current @ V_{OH} = 99.6V	340	410	µA
Maximal frequency @ 32pF	1.93	1.10	MHz

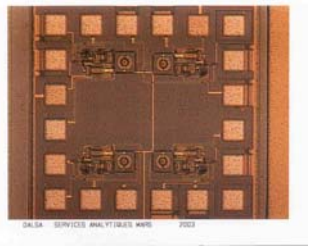

Figure 8 – Micro-photograph of a quad level-up shifter

Conclusion

The digital high voltage interface presented in this paper offers a simple and efficient solution to implement high voltage drivers suitable for telecom, automotive and MEMS applications in a CMOS technology. The level-up shifter circuit acts as an output buffer. It has a measured delay of 200ns when driving a 32 pF capacitive load from a 100V HV power supply. The $\partial V/\partial t$ slope on output was found to be invariant with the supply voltage over a wide range (5V to 100V supply) while the circuit maintained its functionality. When combined with special ESD HV protection devices, 1.5kV HBM was measured. This circuit can be used for any application where a HV driver is needed in the 5V to 100V range. As a cell, this IP core interface is easy to use in any application where a HV driver is needed. The technology used to implement the reported driver is fully characterised for 300V operation, and breakdown voltages over 600V have been routinely measured. Thus the proposed concept can be adapted to implement drivers with much higher supply voltages.

References

[1] M.Y.Park, J.Kim, D.W.Lee, J.S. Park, K.I.Cho, H.J.Cho M.Y. Park, "*A 100V, 10mA High-Voltage Driver Ics for Field Emission Display Applications"*, Korea, Korea, pp.4.

[2] Wen-Tai Wang, Ming-Dou Ker, Mi-Chang Chiang, and Chung-Hui Chen, " *Level Shifter for High-Speed 1V to 3.3V Interfaces in a 0.13um Cu-Interconnection/Low-k CMOS technology"*, Hsinchu, Taiwan, pp.4.

[3] H. Ballan, "*Design and optimisation of high voltage analog and digital circuits built in a standard 5V CMOS technology*", IEEE custom integrated circuits conference, CICC, Swiss Federal Institute of technology, Lausanne, Switzerland, 1993. , pp 4.

[4] H.Ballan and M.Declercq, "*High voltage devices and circuits in standard CMOS technologies*", Kluwer Academic Publishers, 1999, p.287.

[5] K.Joe Hass, David F.Cox, "Level Shifting Interfaces for Low Voltage Logic", 9th NASA Symposium on VLSI Design 2000., pp4.

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