Frequency Limitations of First-Order $g_m - RC$ All-Pass Delay Circuits

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***Abstract*—All-pass filter circuits can implement a time delay but, in practice, show delay and gain variations versus frequency, limiting their useful frequency range. This brief derives analytical equations to estimate this frequency range, given a certain maximum allowable budget for variation in delay and gain. We analyze and compare two well-known $g_m - RC$ first-order all–pass circuits, which can be compactly realized in CMOS technology and relate their delay variation to the main pole frequency. Modeling parasitic poles and putting a constraint on gain variation, equations for the maximum achievable pole frequency and delay variation versus frequency are derived. These equations are compared with simulation and used to design and compare delay cells satisfying given design goals.**

***Index Terms*—All-pass filter, bandwidth, delay, filter optimization, frequency range, phase shift, phase shifter, true time delay.**

I. Introduction

ANALOG time delay circuits have several applications, for instance, compensating delay differences between signal paths, broadband beamforming [1], and equalizing the communication channel for wireline communication [2]. Ideally, such delay circuits should have both a constant unity gain and a well-defined constant delay, which does not vary with frequency. However, practical delay circuits do show frequency-dependent gain and delay variations. This frequency dependence affects the functionality of systems, which exploit delay circuits, limiting their accuracy. For example, in time-delay-based phased-array antenna systems, a frequency-dependent time delay causes frequency dependence in the beam direction ("beam squint") [3], [4].

CMOS is often the desired technology for the implementation of mixed-signal systems. At radio frequencies, operational amplifiers are impractical, and time delays are typically implemented either in transmission lines [5], LC delay lines [1], or all-pass $g_m - RC$ delay circuits [2], [6], [7]. In this brief, we focus on circuits that can be implemented in standard CMOS integrated circuit technology at low area cost and low supply voltage. Transmission lines in CMOS require very long (lossy) metal lines to produce a significant amount of delay, whereas LC delay lines need on-chip inductors. The $g_m - RC$ all-pass delay circuits proposed in [2], [6], and [7] can produce a given amount of delay much more compactly than inductor-based delay cells. Although many tradeoffs exist, for instance, in achievable frequency, noise, linearity, and power consumption, $g_m - RC$ all-pass circuits are clearly area and, hence, cost effective and will be the focus of this brief.

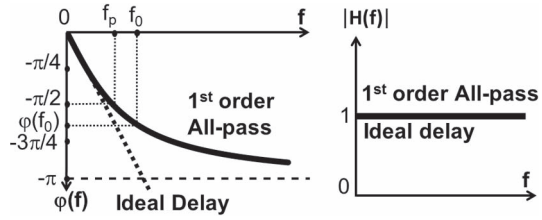

Fig. 1. Phase and gain of an ideal versus first-order delay cell.

An ideal first-order all-pass filter has a pole and zero and can be written as

$$H(s) = \frac{1 - \frac{s}{2\pi f_P}}{1 + \frac{s}{2\pi f_P}} \tag{1}$$

where f_P refers to the pole frequency. Note that the pole and zeros are positioned at $+/-f_P$, resulting in twice the phase and delay of a single-pole system. In addition, the gain is 1 and is frequency independent. Fig. 1 shows the phase and gain of (1), in comparison to an ideal time-delay cell. The time delay at an operating frequency of f_0 is equal to $\tau = -\varphi(f_0)/(2\pi f_0)$. As Fig. 1 shows, the delay of a first-order all-pass cell is frequency dependent and varies with f_0.

In general, delay [8] and gain variations limit the useful frequency range. What is acceptable depends on system requirements (see, for instance, [3] and [4]), and we will assume a maximum allowed gain and delay variation budget. This brief provides a method to analyze the achievable frequency range of delay circuits, given such a budget.

In the literature, we found several delay circuits but no comparison of their relative merits nor a design method to maximize the useful frequency range. This brief aims at filling this gap.

As low-level circuit details critically affect delay cell performance, we will analyze and compare two well-known voltage-mode all-pass circuits. One is the "classical" all-pass delay circuit described in [6], but with much older roots at least dating back to [9]. We will compare this with the "Buckwalter" cell structure proposed in [2]. The circuit in [7] is not considered further, as it is a current-mode circuit complicating comparison and uses three stacked transistors that are less suitable for low supply voltages.

We will propose an analysis method that also holds for the practical case where a delay cell operates in a cascade of similar

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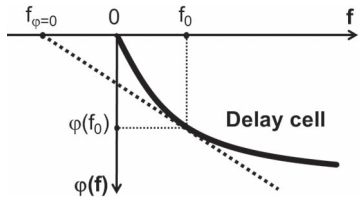

Fig. 2. $f_{\varphi=0}$ for a delay cell with operating frequency f_0.

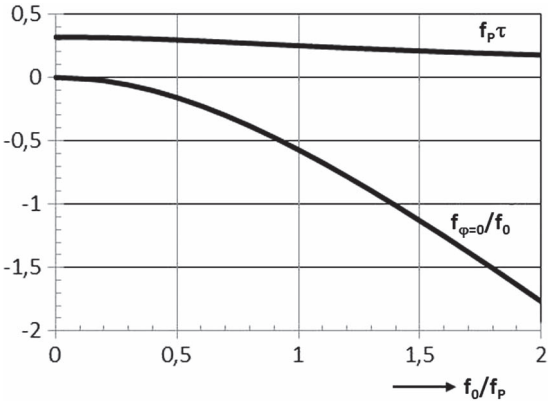

Fig. 3. $f_{\varphi=0}/f_0$ and $f_P\tau$ versus normalized frequency f_0/f_P.

delay cells. The input impedance of the next cell will then load the previous one, while an extra capacitive load (C_L) may also be present. The analysis partly builds on [8], where criterion $f_{\varphi=0}$ is introduced to quantify variations of delay versus frequency. This figure of merit has some properties [8] that we will exploit, which are briefly summarized below.

As shown in Fig. 2, $f_{\varphi=0}$ is the frequency where the tangent to the phase transfer function at f_0 crosses the frequency axis $(\varphi = 0)$. For an ideal time delay cell, $f_{\varphi=0}/f_0 = 0$, and for an ideal phase shifter, $f_{\varphi=0}/f_0 = -\infty$ [8]. For a practical delay cell with a nonlinear phase transfer function, a low value of $f_{\varphi=0}/f_0$ is desirable. In general, $f_{\varphi=0}/f_0$ values can be found from the phase transfer function as [8]

$$\frac{f_{\varphi=0,\text{cell}}}{f_0} = 1 - \frac{\frac{\varphi_{\text{cell}}(f_0)}{f_0}}{\frac{\partial \varphi_{\text{cell}}(f)}{\partial f}\Big|_{f_0}}. \tag{2}$$

Now, relative delay variation $\Delta t_D/t_D(f_0)$ for frequency variation Δf around f_0 is given by [8]

$$\frac{\Delta t_D(f_0)}{t_D(f_0)} \approx \frac{\frac{f_{\varphi=0,\text{cell}}}{f_0}}{1 - \frac{f_{\varphi=0,\text{cell}}}{f_0}} \frac{\Delta f}{f_0}. \tag{3}$$

Clearly, if $(f_{\varphi=0}/f_0) \ll 1$, then $\Delta t_D/t_D(f_0) \approx 0$, which means that the circuit approximates an ideal delay over frequency band Δf.

If we apply (2) to the phase transfer function of the ideal first-order all-pass cell (1), we find

$$\frac{f_{\varphi=0,\text{cell}}}{f_0} = 1 - \frac{a\tan(f_0/f_p)}{f_0/f_p}\left(1 + (f_0/f_p)^2\right). \tag{4}$$

Fig. 3 plots numerical values for (4) versus operating frequency f_0, normalized to pole frequency f_p. In addition, $f_P\tau$ is shown, which slightly varies around 0.25 for $f_0 = f_p$ (phase shift $-\pi/2$). For low relative delay variation at given Δf and f_0, (3) asks for low $f_{\varphi=0}/f_0$, i.e., large f_P. However, as $f_P\tau$ is around 0.25, less delay per cell results (roughly $\propto 1/f_P$). Fortunately, cascading cells allows for more delay at constant relative delay variation. If cells are identical, $f_{\varphi=0}$ of the cascade is equal to that of a cell [8]. Hence, analyzing f_p of a single (loaded) cell is sufficient to characterize a cascade of delay cells with respect to delay variation.

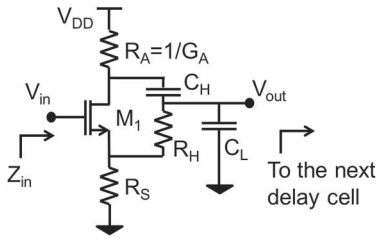

Fig. 4. "Classical" first-order all-pass delay cell.

In this brief, we will show how the maximum value of f_P is limited by the circuit topology and technology parameters, where also gain variations induced by parasitic poles will be considered. Note that previous work [8] only modeled ideal low-pass RC and LC delay cell behavior, no all-pass cells. Moreover, no gain variation effects nor parasitic loading effects were modeled, which is way too optimistic.

The maximum achievable f_p will now be analyzed for the "classical" delay circuit in Section II and the "Buchwalter" delay circuit in Section III. Section IV will verify analysis by simulation and compare the relative merits of the circuits. Section V will present the conclusions.

II. Analysis: The Classical Delay Circuit

Fig. 4 shows the classical all-pass delay cell [6], [9]. Instead of resistors, diode-connected MOSFETs or triode MOSFETs may also be used; however, resistors are preferred for linearity reasons, for having less parasitic capacitance than MOSFETs, and for requiring low voltage headroom.

Equation (5) shows an approximate transfer function, i.e.,

$$\frac{V_{\text{out}}}{V_{\text{in}}} \approx \frac{g_m}{g_m + G_A} \cdot \frac{1 - R_H C_H s}{1 + \left(R_H + \frac{2}{g_m + G_A}\right)(C_H + C_{\text{in}} + C_L)s}. \tag{5}$$

C_{in} is the input capacitance of the next stage. If each delay cell is cascaded with identical delay cells, then $C_{\text{in}} \approx 2C_{\text{gd}}$ (due to the Miller effect on C_{gd}). Equation (5) differs from transfer function (1) because its dc gain is less than one and the absolute value of the pole and zero differ from each other, causing attenuation at high frequencies (see Fig. 5). Still, (5) can approximately imitate transfer function (1); hence, we can reuse (4) provided that two conditions are satisfied as follows:

1) $(g_m/g_m + G_A) \approx 1$;
2) $(R_H + 2/(g_m + G_A))(C_H + C_{\text{in}} + C_L) \approx R_H C_H$.

The second condition ensures proximity of the absolute value of the pole and the zero frequency, which keeps the amount of frequency-dependent gain attenuation small.

We will now assume that the design requirements are

1) dc gain $A_{v0}, (0 < A_{v0} < 1)$;
2) high-frequency attenuation $\leq \Delta H_p$.

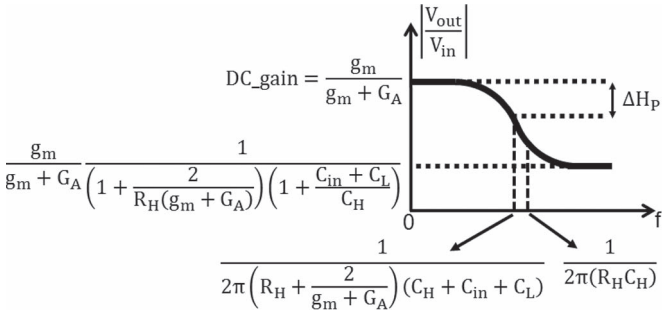

Fig. 5. Voltage gain of the "Classical" delay cell.

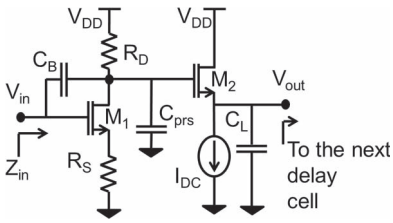

Fig. 6. Buckwalter circuit.

By substituting these values in (5), we get

$$R_A \geq \frac{A_{V0}}{1-A_{V0}}\frac{1}{g_m} \tag{6}$$

$$R_H \geq \frac{2A_{V0}}{g_m\left(\frac{1}{\sqrt[4]{2(1-\Delta H_p)^2-1}-1}\right)} \tag{7}$$

$$C_H \geq \frac{C_L+2C_{gd}}{\left(\frac{1}{\sqrt[4]{2(1-\Delta H_p)^2-1}}-1\right)}. \tag{8}$$

Based on (7) and (8), the condition on the pole and zero frequencies for the "Classical" delay circuit becomes

$$|f_{p,C}| \leq \frac{1}{2\pi R_H C_H}\cdot\sqrt[2]{2(1-\Delta H_p)^2-1} \tag{9a}$$

$$|f_{z,C}| \leq \frac{1}{2\pi R_H C_H}. \tag{9b}$$

Note that (9a) gives the maximum possible pole frequency, i.e., the lowest delay variation [see (4) and Fig. 3].

III. Analysis: The Buckwalter Delay Circuit

Fig. 6 shows the all-pass circuit proposed by Buckwalter [2] implemented using MOSFETs and resistors.

As aforementioned, the circuit is cascaded with identical circuits; therefore, the circuit is loaded with impedance that is equal to its input impedance and an extra load capacitance C_L. The input impedance can be simply approximated by evaluating the Miller effects on capacitance values C_B and $C_{\rm gs1}$: $C_{\rm in}\approx 2C_B+C_{\rm gs1}/(1+g_mR_S)\approx 2C_B$. During the rest of the calculations, the value of $C_{\rm gd1}$ is absorbed inside C_B. $C_{\rm prs}=C_{\rm db1}+C_{\rm gd2}$. The approximate transfer function of the circuit is

$$\frac{V_{\rm out}}{V_i} \approx -\frac{R_D}{\frac{1}{g_{m1}}+R_s}\cdot\frac{1-\frac{1+g_{m1}R_s}{g_{m1}}C_Bs}{1+R_DC_B\left(1+\frac{2}{R_Dg_{m2}}\right)\left(\frac{1+\frac{C_{prs}}{C_B}+\frac{C_L}{C_B}\frac{1}{R_Dg_{m2}}}{1+\frac{2}{R_Dg_{m2}}}\right)s}. \tag{10}$$

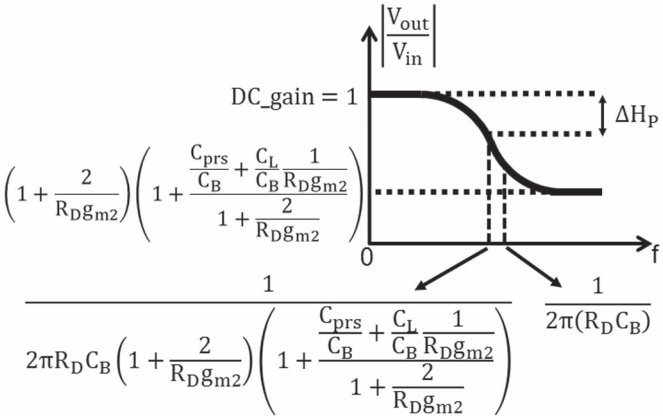

Fig. 7. Voltage gain of the Buckwalter delay cell.

The right side of (10) contains two parts. The first part is the dc gain, and the second part is approximately the all-pass transfer function. The initial phase shift at dc is π, which we do not consider in our calculations because in processing differential signals, the π phase shift can be compensated with interchanging the output signals [2]. To design the delay circuit, we again aim at approximating transfer function (1). For the unity dc gain, the following condition must be satisfied: $R_D = R_S + 1/g_{m1}$. Fig. 7 shows the gain transfer function of the Buckwalter delay circuit with unity dc gain.

Equation (10) can approximate the transfer function of an all-pass delay cell, provided that two conditions are satisfied, i.e.,

$$\frac{\frac{C_{prs}}{C_B}+\frac{C_L}{C_BR_Dg_{m2}}}{1+\frac{2}{R_Dg_{m2}}} \ll 1 \quad \text{and} \quad \frac{2}{1+R_Dg_{m2}} \ll 1.$$

These conditions cause the absolute values of pole and zero to be close to each other. Suppose there are two design requirements: 1) dc gain $= 1$ and 2) at $f_0 = f_P$, the high-frequency attenuation $\leq \Delta H_p$. Via these assumptions, we can find g_{m2}, C_B, and f_p. Thus

$$g_{m2} \geq \frac{2\left(\sqrt[4]{2(1-\Delta H_P)^2-1}\right)}{\left(\frac{1}{g_{m1}}+R_s\right)\left(1-\sqrt[4]{2(1-\Delta H_p)^2-1}\right)} \tag{11}$$

$$C_B \geq \frac{\left(C_{prs}+\frac{C_L}{R_Dg_{m2}}\right)}{1+\frac{2}{R_Dg_{m2}}}\frac{\sqrt[4]{2(1-\Delta H_P)^2-1}}{1-\sqrt[4]{2(1-\Delta H_P)^2-1}}. \tag{12}$$

Substituting $R_D = (1/g_{m1}) + R_s$ (the unity gain condition), g_{m2}, and C_B in (10) results the following pole and zero conditions:

$$|f_{p,B}| \leq \frac{1}{2\pi R_DC_B}\sqrt[2]{2(1-\Delta H_p)^2-1} \tag{13a}$$

$$|f_{z,B}| \leq \frac{1}{2\pi R_DC_B}. \tag{13b}$$

Again, (13a) provides an estimate of the maximum possible pole frequency of the Buckwalter delay circuit, and (3) and (4) and Fig. 3 relate this to delay variation.

TABLE I
TRANSISTOR DESIGN PARAMETERS USED

Circuit	W/L [µm/µm]	$V_{GS,OV}$[mV]	f_T [GHz]
"Classical"	420.76/0.24	75	12.4
Buckwalter	$(W/L)_1$=26.29/0.24 $(W/L)_2$=394.46/0.24	75	12.4

IV. VERIFICATION AND DESIGN EXAMPLES

To verify analysis and exemplify how the analytical equations can be used during design, we will address two design questions as follows: 1) Which of the delay cells achieves the highest f_p for a given power budget? and 2) What is the power consumption for each delay circuit provided that they fulfill the same delay and noise figure requirements?

We will use a CMOS process UMC 180-nm supply voltage that is equal to 1.8 V.

A. Maximum f_p for a Given Power Budget

Suppose the design requirements for a delay cell in a cascaded chain are dc gain > -1 dB and $\Delta H_p < 1$ dB, and we allow a maximum dc current of 3.5 mA. Assume also two loading cases: C_L is 0 or 2 pF. We aim at finding the best circuit w.r.t. delay variations and, hence, compare the maximum achievable f_P. To reduce the channel length modulation in transistors, their lengths are chosen to be 240 nm. The overdrive voltage of all transistors is chosen equal for both circuits ($V_{\mathrm{GS,OV}} = 75$ mV), so that f_T of the transistors is equal. For Buckwalter's cell, the size of M_2 is chosen to be ≈15 times of M_1 to satisfy (11), even for $R_s = 0$ (see Table I).

For these transistor sizes, C_{gd} for "Classical" is 173 fF, and C_{prs} for "Buckwalter" is around 152 fF. Based on (8) and (12) and $C_L = 0$, we find $C_H \geq 2434$ fF and $C_B \geq 943$ fF, whereas for $C_L = 2$ pF, we find $C_H \geq 16.508$ pF and $C_B \geq 1.771$ pF. (In the Buckwalter circuit, the effect of C_L is reduced by the buffer stage.) The values for resistors calculated based on (7) are $R_A = R_S = 170\ \Omega$ and $R_H = 252\ \Omega$, whereas for the Buckwalter circuit, we find $R_S = 0$, $R_D = 249\ \Omega$ (to have unity gain condition at dc: $R_D = R_S + 1/g_{m1}$. Table II shows calculated and simulated values for each delay cell for the two loading conditions, which match good enough for first-cut circuit design. As noise and linearity are often also important, we also added simulation results for noise and $\mathrm{IIP_3}$ (with 50 Ω as reference) for operating frequency ≈ f_p, where ΔH_p has been estimated and verified. Overall, the Buckwalter cell achieves better higher f_p and is less sensitive to C_L.

Fig. 8 shows the simulated phase and gain plots of the delay cells. The values of A_{V0} (the dc gain) and ΔH_p (gain drop at the pole frequency) are shown in the figures, where the pole frequency is defined as the frequency where the phase has dropped 90° with respect to dc. Note that, although circuit parasitics affect the transfer function, the phase characteristic roughly resembles that of a first-order all-pass filter. As predicted, the "Classical" circuit has attenuation at low frequency, but the Buckwalter circuit can have quite near to unity dc gain. Clearly, the Buckwalter circuits achieve the best frequency range, with also less overall attenuation.

TABLE II
COMPARISON OF THE DELAY CELL PROPERTIES

	Classic 0 fF	Classic 2pF	Buckw. 0 fF	Buckw. 2pF
C_L [pF]	0	2	0	2
I_{DC} [mA]	3.5	3.5	3.5	3.5
#NMOS	1	1	2	2
$f_{T,NMOS}$ [GHz]	12.4	12.4	12.4	12.4
ΔH_p calc. [dB]	1	1	1	1
ΔH_p sim. [dB]	1.29	0.84	1.25	0.97
A_{vo} calc. [dB]	-1	-1	0	0
A_{vo} sim. [dB]	-1.47	-1.47	-0.28	-0.28
f_p calc. [MHz]	199	29.3	520	277
f_p sim. [MHz]	201	32.2	546	288
$\sqrt{\overline{V_{n,in}^2}}$ $[\frac{nV}{\sqrt{Hz}}]$	2.7	2.7	2.4	2.4
$\mathrm{IIP_3}$ [dBm]	16.5	17.5	14.8	17

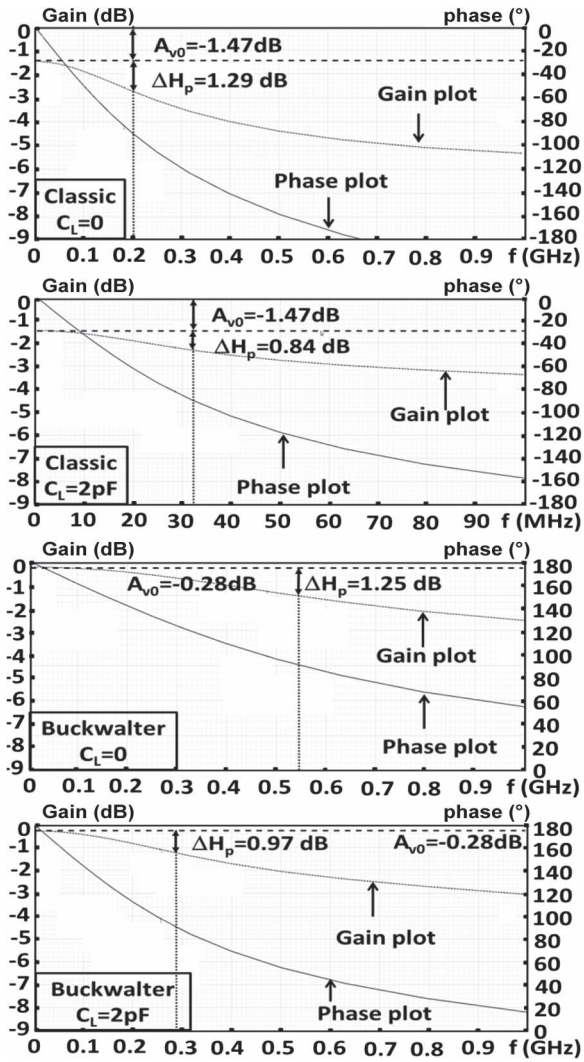

Fig. 8. Simulated phase and gain for $C_L = 0$ and $C_L = 2$ pF.

If we compare these results with that of a single-pole low-pass circuit, we achieve double the delay using an all-pass cell and about a 1-dB gain drop instead of 3 dB at the pole frequency.

TABLE III
PARAMETERS FOR EQUAL DELAY AND 10-dB NOISE FIGURE

	W/L [μm/μm]	V_{ov} [mV]	f [GHz]	I_{bias} [mA]	Total I [mA]
"Classical"	412.45/0.24	75	12.4	3.43	3.43
"Buckwalter"	20.37/0.24	75	12.4	0.17	2.71
	305.78/0.24	75	12.4	2.54	

B. Power Comparison for Equal Delay Cell Requirements

Suppose now the following properties are desired: an operating frequency $f_0 = 100$ MHz, a relative delay variation of 5% for $\Delta f = \pm 10$ MHz around f_0, a dc gain of > -1 dB, $\Delta H_p < 1$ dB, and NF $= 10$ dB referred to 50 Ω, while we want to calculate the achievable delay per cell.

To obtain the maximum delay per cell, we choose the minimum f_p that just satisfies (3) [8] for the aforementioned requirements. For design, suppose the initial sizes of the transistors are as in Table II, then from f_p, we find the value of capacitors. Using admittance scaling [10] to satisfy the noise figure requirements, we multiply all W and capacitor values by α and divide all resistor values by α. With this method, the circuit delays do not change; however, the noise figure will change proportional to the power consumption (constant signal-to-noise ratio/Power [10]). The power consumption also strongly depends on the overdrive voltage of the transistors. Substituting the delay variation of 5% and relative bandwidth of ± 10 MHz into (3) results in $f_{\varphi=0}/f_0 = -1$. In the graph in Fig. 3, this corresponds to $f_0/f_p = 1.4$. Therefore, the minimum value of f_p of the delay cells must be $100/1.4 = 71.4$ MHz. This requires equal f_P for both circuits, i.e., $R_H C_H \approx 1/2\pi f_p = 2.23e-9$ and $R_D C_B \approx 1/2\pi \mathrm{f}_p = 2.23e-9$. To bring the noise figure to 10 dB for both, the values of resistors and capacitors will be $R_A = R_S = 173.4\ \Omega$, $R_H = 257\ \Omega$, $C_H = 8.67$ pF and $R_s = 0$, $R_D = 321.2\ \Omega$, $C_B = 6.94$ pF. Table III shows the resulting aspect ratio and dc consumption of both circuits. The achievable delay with both circuits now is 3.025 ns at $f_0 = 100$ MHz. For the same noise figure, the Buckwalter cell consumes 20% less dc than the Classical circuit. In addition, the majority of its current is mainly consumed by the buffer transistor. For some applications, the loading capacitance may be small, and it might be possible to remove the buffer part of the Buckwalter circuit to reduce its power consumption.

V. SUMMARY AND CONCLUSION

A method for analyzing the maximum useful frequency range of first-order all-pass delay cells has been introduced. It has been used to analyze and compare two well-known $g_m - RC$ delay cells, i.e., the "Classical" and the "Buckwalter" all-pass cell. The analysis holds for single and cascaded identical cells. To this end, the cells have been analyzed as a self-loaded content with an arbitrary extra loading capacitance. The resulting transfer function deviates from ideal delay-cell behavior in two key aspects, i.e., both the gain and delay are frequency dependent. Design boundary conditions were derived for each all-pass circuit to keep the gain variation below a specified maximum and ensure that the shape of the transfer function still resembles the simple first-order all-pass function (1), which is characterized by one pole frequency f_P. The design boundary conditions were then expressed as constraints on the maximum achievable pole frequency f_P. Substituting f_P in (4), (3) can now be used to estimate the amount of delay variation as a function of frequency variation Δf around nominal operating frequency f_0.

For any single first-order all-pass delay cell, or approximation thereof, a larger value of f_p renders smaller delay variations over a given frequency range Δf around f_0, but also smaller delay (see Fig. 3). When cascading multiple cells, each cell needs to realize less delay and, hence, can have higher f_P, resulting in less relative delay variations (3). This thus results in a larger useful frequency range (but more chip area and power consumption). The equations in this brief model the tradeoffs between delay-cell pole frequency f_P, center frequency f_0, frequency range Δf, and delay variation, while keeping amplitude variations within a budget and allowing for improving performance by cascading cells.

To exemplify the usefulness of the analysis, it was applied to two delay cells to compare their relative performance and estimate their delay variation versus frequency. With the help of the derived design equations, an optimization of f_p was illustrated, keeping delay and power constraints fixed, comparing results with and without extra capacitance. Then, the analysis results were exploited to achieve equal delay with different circuits, under the condition of fixed noise performance, while comparing power dissipations. Similar analysis can be done for other kinds of first-order $g_m - RC$ all-pass delay cells.

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