4.4 A 1-to-2.5GHz Phased-Array IC Based on g_m-RC All-Pass Time-Delay Cells

Seyed Kasra Garakoui, Eric A.M. Klumperink, Bram Nauta, Frank F.E Van Vliet

University of Twente, Enschede, The Netherlands

Electronically variable delays for beamforming are generally realized by phase shifters. Although a constant phase shift can approximate a time delay in a limited frequency band, this does not hold for larger arrays that scan over wide angles and have a large instantaneous bandwidth. In this case true time delays are wanted to avoid effects such as beam-squinting. In this paper we aim at compactly integrating a delay based phased-array receiver in standard CMOS IC technology. This is for instance relevant for synthetic aperture radars, which require large instantaneous bandwidths often in excess of 1GHz, either as RF or as IF bandwidth in a superheterodyne system. We target low-GHz radar frequencies, assuming sub-arrays of four elements and up to 550ps delay.

Integrated time-delay cells have been proposed based on the approximation of transmission-line segments with integrated LC lumped elements [1]. These, however, require bulky on-chip inductors. A gm-RC or gm-C all-pass delay circuit [2,3] can produce a given amount of delay in a much smaller area. This paper proposes an improved gm-C delay cell that realizes an accurate integrated time delay over a wide (1 to 2.5GHz) frequency band, at an acceptable power dissipation. With these wideband time-delay cells, a 4-element phased-array receiver front-end was designed in 0.14 µm CMOS.

Figure 4.4.1 shows the architecture of the 4-element phased-array receiver front-end IC. The four received signals are first amplified by an LNA with differential output [4], which takes care of a broadband 50 W matching to the antennas. This matching is important to reduce mutual coupling between adjacent antenna elements. The LNA is followed by a delay chain which is subdivided into fine and coarse delay cells, of which several are cascaded. The desired delay in path *i* is coarsely selected via control signals $C_{i,0}..C_{i,4}$, which actives one particular V-I converter. The delay is then adjusted by setting the delay of the fine-tune bits via the $\Delta\tau$ control bits. The output signals of the four active V-I converters (one per channel) can now be added in the current domain, in which the effective beamforming takes place. The summed signals are downconverted in a mixer. The mixer is loaded with an output buffer that provides 50Ω matching at the output of the IC. Provisions to measure or use the time-delayed signal before downconversion are also implemented.

The use of known time-delay cells turned out to add unacceptable dispersion. A new time-delay circuit was designed based on the H(s) expression shown in Fig. 4.4.2. This all-pass transfer function features a delay $t_D = 2C/g_{mp}$. This transfer function is realized by two parallel paths: a unity gain path (G_1R_L=1) and a first-order low-pass filter, designed for a gain of two ($G_2R_1G_3R_L$=2) and pole at $1/R_1C=g_{mp}/C$. Implementing the capacitor as a variable capacitor allows for delay control. On the transistor level G_1, G_2, G_3, R_1 and R_L are realized by M_1,M_2,M_5,M_4 and M_3 respectively. The capacitor was implemented both fixed (for the coarse-tune bits) and variable (for the fine-tune bits). The fine control was implemented by means of 3 binary weighted capacitors (3b resolution), while coarse control involves selecting another output (see Fig. 4.4.1).

Features of this time-delay cell include an accurately adjustable delay (by C), low delay variation versus frequency and an accurately controllable unity gain.The DC-coupled nature allows for cascading cells without DC-blocking capacitors. The circuit works down to low supply voltages and exploits current re-use to limit dissipation. Comparison to [2,3] in the same technology shows a better delay approximation over a wider bandwidth, especially because floating capacitors are avoided, removing the most significant parasitic poles. The remaining parasitic pole at the output was shifted up by inductive peaking via active inductors (resistor in the gate line to M3, not shown for simplicity).

As shown in Fig. 4.4.1, control bits $C_{i,1}$-$C_{i,4}$ active one V-to-I converter to select a delay. Summation of the signals of different antenna channels is performed in the current domain. At every delay setting, only a single V-to-I converter is active per channel, leading to small and equal extra delay in all four channels (i.e. no differential delay error). An active mixer implements frequency downconversion, where the sum of the V-to-I converter currents is injected as RF tail current to a switching pair. In order to keep the frequency scheme flexible, the local oscillator signal is provided off-chip.

The main feature of the realized RFIC, its time delay, was characterized over all coarse and fine delay setting combinations over a wide frequency range. The results are shown in Fig. 4.4.3. For a bandwidth of more than 1.5 GHz (1 to 2.5GHz), the delay variation is less than ±10ps. Note that this is achieved without calibration. At the same time, the gain variation is as low as ±0.4dB.

Figure 4.4.4 shows the gain, noise figure and S_{11} of a single channel consisting of the LNA, balun, and delay line at maximum delay. The gain roll-off is introduced in the LNA with balun, ironically by parasitics of the only remaining floating DC-blocking capacitor (that were avoided in the delay cell). Although significant, the effect is again identical for all channels, and does not ruin normalized beam patterns. Gain and matching compare well to literature (see Fig. 4.4.6), but noise is still a bit on the high side. Note that the noise figure is delay dependent (between 8dB and 10dB). The reported values are for the worst case delays.

In Fig. 4.4.5, a comparison between the measured beam pattern of our IC and a simulated ideal pattern for 4 antennas with ideal time delays is shown. Results for operating frequencies at 2.0 and 2.5GHz are shown; the time-delays were tuned to get a pointing angle of +60° at 2.5GHz. The incident signal was generated by a single RF signal generator and a 1-to-4 power splitter, to avoid practical antenna issues. The LO frequency is chosen to be 3GHz, downconverting the frequency band of 2 to 2.5 GHz to 0.5 to 1.0 GHz. Figure 4.4.5 demonstrates that the spatial beam direction closely resembles the ideal system response. No beam-squinting is visible even for 500MHz frequency difference ($\Delta f/f$=20%). The same is true for the position of the nulls (null-depth is limited by the limited isolation between PCB RF signal tracks to the IC).

Figure 4.4.6 compares our IC with other time-delay beamforming ICs [1,5]. The occupied area is an order of magnitude smaller than results from the literature, whilst the integrated delay is significantly larger. The relative area is hence at least an order of magnitude better. The same holds for the delay flatness. This flatness is comparable to the resolution, but for more delay and at a lower frequency. Gain variation is also better. Note that these results are obtained without calibration. Delay steps are uniform and monotonously increasing, which facilitates easy control and avoids intricate lookup tables and calibration schemes.

Acknowledgements:
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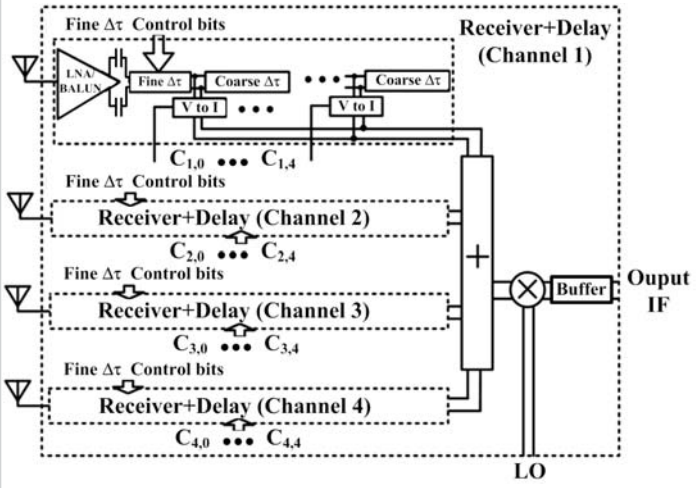

Figure 4.4.1: Block diagram of the 4-channel IC.

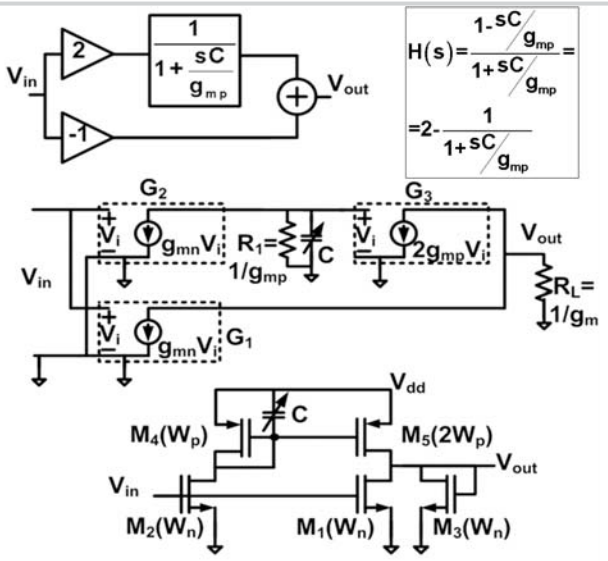

Figure 4.4.2: Delay cell block and circuit diagrams.

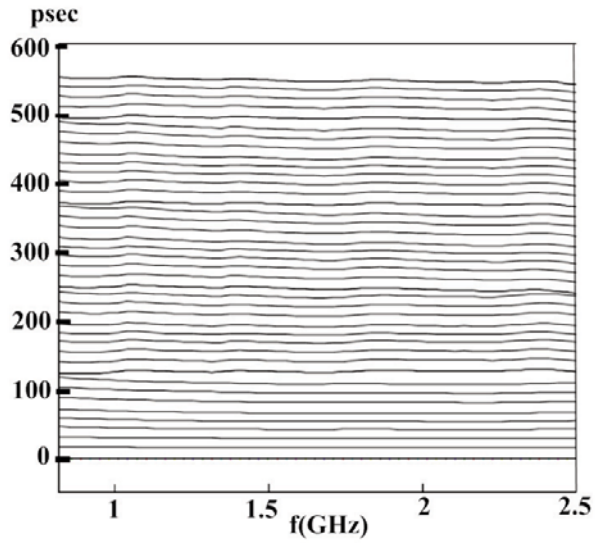

Figure 4.4.3: Measured delay for all delay settings.

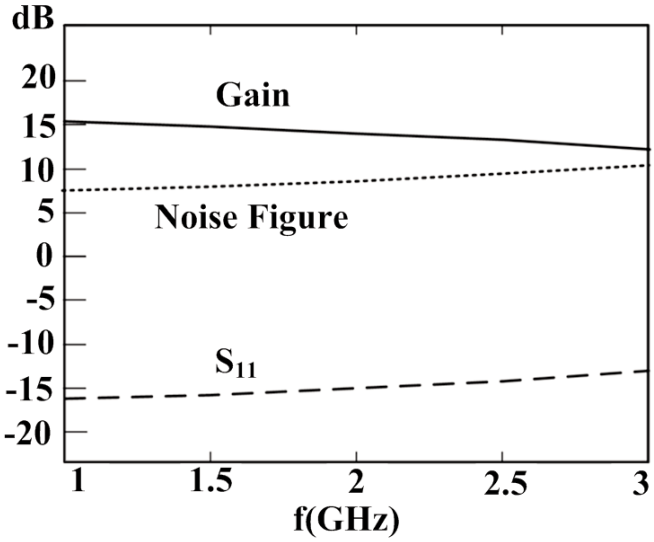

Figure 4.4.4: Gain, $S_{11}$and Noise Figure per channel.

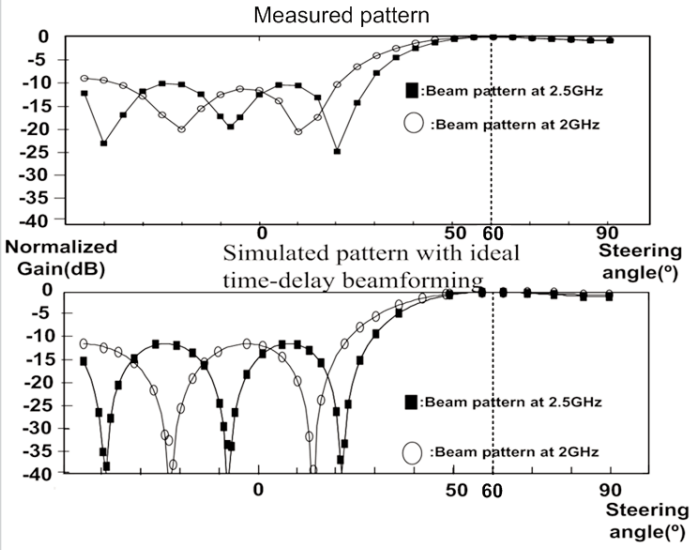

Figure 4.4.5: Beam patterns for 60° beam direction.

	This work	[1]	[5]
Technology	140nm	130nm	250nm PHEMT
Technique	G_m-C	LC delay	MMIC integrated delay line
Features per antenna channels			
Gain	15dB	10dB	6-9dB
Noise Figure	8-10dB	2.9-4.8dB	4.3dB
IIP3	-13dBm	Not mentioned	Not mentioned
-1dB compression point	-21dBm	Not mentioned	5dBm
Amplitude variation vs.f	±0.4dB	±1dB	±2.5dB
Delay resolution	14psec	15psec	2.5psec
Delay variations vs. f	<10psec	<40psec	<20psec
Maximum delay	550psec	225psec	150psec
Power consumption	50mA	40mA	Not mentioned
Complete 4 channel wide band beamformer			
Beam direction resolution	4.7Bit	3.5 Bit	6 Bit
Bandwidth	3GHz	18GHz	3-16GHz
Power consumption	250mA@1.8V	370mA@1.5V	Not mentioned
Die area	1mm²	10mm²	10mm²

Figure 4.4.6: Performance overview and comparison.

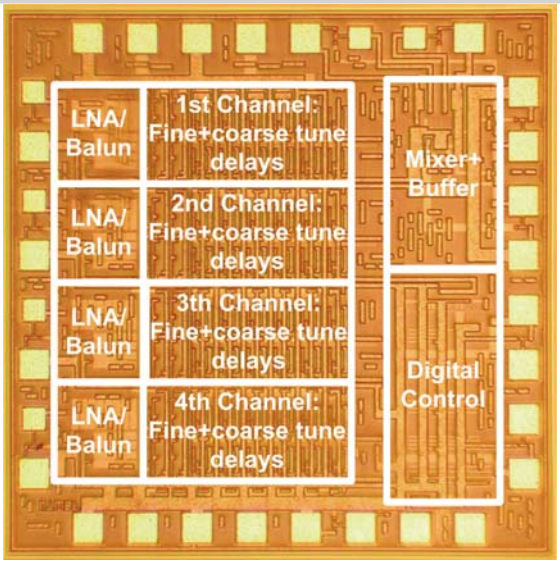

Figure 4.4.7: Photograph of the chip, measuring 1.0×1.0mm².

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