AXIOM_PWMMOD256fs1b
256fs – 1bit PWM sigma-delta modulator

Features
- 117 dB dynamic range
- -120 dBFSA in-band noise
- ISI insensitive bit stream
- No signal dependent kick back on DAC reference
- Multi bit advantages with a single bit modulator
- Hardware costs ~ 700 gates
- 0.018 mm² in 0.14μm CMOS
- Silicon proven

Applications
- High accuracy PCM to PWM conversion
- Signal generation for Class-D amplifiers
- D/A converters
- Audio subsystems
- Audio amplifiers with digital inputs
- Ideal in combination with FIRDAC (114dB DR measured)
- FPGA solution with discrete DAC (110dB DR measured)

Description
A PWM sigma-delta modulator is a special type of 1-bit sigma-delta modulator that produces a pulse width modulated (PWM) output signal with a fixed repetition frequency. A fixed repetition frequency makes the output signal insensitive to typical problems associated with (continuous time) sigma-delta converters, such as non-linear inter symbol interference (ISI) and kickback noise on the reference of the DAC.

This IP block implements a digital PWM sigma-delta modulator consisting of a fifth-order loop filter, followed by a 16 taps moving average filter, a sawtooth carrier injection (with a frequency of \(f_{CLK}/16\)) and a 1-bit quantizer. The functional block diagram is shown in Figure 1.

![Figure 1 – Block diagram PWM modulator](image-url)
Proven performance

The PWM ΣΔ modulator was introduced in literature by [DOOR2005]. In that paper, results of a D/A converter show that the PWM ΣΔ modulator enables high audio performance (106dB SNDR\textsubscript{MAX}, 114dB dynamic range, A-weighted) with very simple 1-bit DAC components. That paper also shows that the PWM ΣΔ modulator is very suitable to operate together with a FIRDAC (also known as a 'semi-digital reconstruction filter', see AXIOM_FIRDAC).

In another experiment, with the PWM ΣΔ modulator implemented on an FPGA and a DAC build from common off the shelf (COTS) components (a 74HCT574, 8 resistors, an Op-amp and an RC feedback network), an audio performance of 110dB dynamic range and 97dB SNDR\textsubscript{MAX} was measured.

Detailed description

A functional block diagram of the PWM ΣΔ modulator is shown in Figure 1. It differs from a standard ΣΔ modulator in two ways:

- A digital 16 step sawtooth is added to the output signal of the loop filter to force a PWM output signal with a fixed switching frequency of $f_{CLK}/16$.
- The loop filter is cascaded with a 16-tap FIR interpolation filter to improve loop stability.

The PWM signal has a 4-bit time resolution, corresponding to 16 discrete pulse widths. With the frequency in the modulator loop being $256*f_S$ this results in a PWM frequency of $16*f_S$. The multi bit behavior of the PWM signal at low frequencies has a positive effect on the loop stability. Therefore, aggressive noise shaping can be used, while the modulator remains inherently stable up to high modulation depths. In this realization with a 5\textsuperscript{th} order loop filter, stable behavior is guaranteed up to 85% modulation depth. A spectrum of the output of the PWM ΣΔ modulator with such an input is shown in Figure 2. As in normal sigma-delta modulators, state limiters inside the loop filter enable 100% modulation depth, but with reduced performance, see Figure 3.

Specifications

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>DESCRIPTION</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
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<tbody>
<tr>
<td>TECHNOLOGY</td>
<td>0.14μm CMOS technology</td>
<td>0.14</td>
<td></td>
<td></td>
<td>μm</td>
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<tr>
<td>Area</td>
<td>Chip area in 0.14μm CMOS</td>
<td>0.018</td>
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<td></td>
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<tr>
<td>$N_{GATES}$</td>
<td>Number of gates / hardware cost</td>
<td>700</td>
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<td>FREQUENCIES</td>
<td>Sample frequency</td>
<td>44.1 - 48 kHz</td>
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<td></td>
<td>kHz</td>
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<td>$f_{CLK}$</td>
<td>Clock frequency (input)</td>
<td>256 $f_S$</td>
<td></td>
<td></td>
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<tr>
<td>$f_{PWM}$</td>
<td>PWM frequency</td>
<td>$1/16 f_{CLK}$</td>
<td></td>
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<td>MODULATOR PERFORMANCE</td>
<td>Stopband edge for quantization noise</td>
<td>0.45 $f_S$</td>
<td></td>
<td></td>
<td>dBFS</td>
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<td>$e_{QN}$</td>
<td>Inband quantization noise of the modulator</td>
<td>-116 dBFS, -120 dBFS</td>
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<td>DR</td>
<td>Dynamic range</td>
<td>117 dB</td>
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<tr>
<td>$SNR_{MAX}$</td>
<td>Maximum Signal to Noise Ratio</td>
<td>116 dB</td>
<td></td>
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<tr>
<td>$U_{IN,MAX}$</td>
<td>Maximum input without invoking limiters</td>
<td>-1.4 dBFS</td>
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Table 1 – Specifications of the PWM ΣΔ modulator.
Port list

<table>
<thead>
<tr>
<th>PORT NAME</th>
<th>WIDTH</th>
<th>DESCRIPTION</th>
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<tbody>
<tr>
<td>Clk</td>
<td>1</td>
<td>Clock input, at 256*fs</td>
</tr>
<tr>
<td>Reset_N</td>
<td>1</td>
<td>Reset input (active low), resets all states to initial condition</td>
</tr>
<tr>
<td>PCM_in</td>
<td>24</td>
<td>PCM input, at N<em>fs (as long as N</em>fs is synchronous to Clk)</td>
</tr>
<tr>
<td>PWM_out</td>
<td>1</td>
<td>PWM output</td>
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</table>

Table 2 – Port function description

Typical characteristics

![Power spectrum](image1.png)
![Performance of PWM SD Modulator](image2.png)

Figure 2 – Output power spectrum with -1.4dBFS input and f_s=44.1kHz.

Figure 3 - Modulator performance with f_s=44.1kHz.

Deliverables

The IP deliverable consists of a RTL description in VHDL of the PWM sigma-delta modulator. The product can be delivered as a single IP component for customer integration or Axiom IC engineers can integrate the product as part of a SoC engagement.

**Design unit**: PWM_SD_Modulator (RTL, containing entity and architecture)

**File name**: pwm_sd_modulator.vhd

**Version**: 1.31F or higher

**Target**: Synthesizable as ASIC logic or on FPGA

**Limitations**: None known

**Errors**: None known

**Dependencies**: 1. IEEE.Numeric_Std
                 2. DSP_functions (package that contains general arithmetic routines, will also be delivered)

**Behavioral modeling**: RTL code is suitable for behavioral simulations, other types of behavioral models can be delivered upon request.

**Samples**: bit stream examples are available for experimentation.
References


Revision history

<table>
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<tr>
<th>REVISION</th>
<th>DATE</th>
<th>REASON FOR REVISION</th>
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<tr>
<td>F4</td>
<td>2014-10-08</td>
<td>Initial version in Teledyne template; port from old datasheet format</td>
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<tr>
<td>D5a</td>
<td>2014-12-04</td>
<td>Corrected header, logos, last page links</td>
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Table 3 – Document revision history